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EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,075	AZEVEDO ET AL.	
	Examiner	Art Unit	
	Emerson C. Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is made **Non-Final**.

Claims 1-28 have been examined.

Claim Objections

Applicant is advised that should claims 2 and 3 be found allowable, claims 8 and 9, respectively will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claims 1-28 are objected to because of the following informalities:

In regards to claims 1,7,13,19, and 25-28, please change "the error recovery"(see last line of claims) to "the error recovery instruction". The limitation "the error recovery" lacks antecedent basis.

In regards to claim 27, please change "the timer"(see line 5) to "a timer". The limitation "the timer" lacks antecedent basis.

The remaining claims, not specifically mentioned, are objected because they are dependent upon one of the claim above.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13-18 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "the timer" in line 3 of claim. There is insufficient antecedent basis for this limitation in the claim. A "timer" is disclosed later in the claim (see line 5). Examiner suggests amending "the timer" as cited in line 3 of claim to "a timer" and amending "a timer" as cited in line 5 of claim to "the timer".

The remaining claims, not specifically mentioned, are rejected because they are dependent upon the claim above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3,6-9,12-15,18-21, and 24-28 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,345,392 of Mito et al. referred hereinafter Mito.

In regards to claims 1 and 7, Mito discloses a program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions

executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction. Mito discloses receiving an interrupt (see figure 4 and column 8 lines 36-37).

beginning a timeout task. Mito discloses a watchdog timer (see figure 4 item 172 and column 8 lines 36-37).

monitoring processor status to determine a time to perform the error recovery instruction Mito discloses monitoring for interrupts to initiate a suspend routine (see figure 4 and column 8 lines 25-30 and 45-47).

performing the error recovery instruction when the monitoring determines a time for performing the error recovery Mito discloses initiating a suspend routine (see column 8 lines 45-47).

In regards to claim 2 and 8, Mito discloses the claim limitations as discussed above. Mito further discloses forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction. Mito discloses high temperatures and low battery, which could represent time to perform error recovery instructions (see figure 4 items 174,176 and column 8 lines 25-30). Mito further discloses a watchdog timeout, indicating a timeout task (see figure 4 item 172 and column 8 lines 25-30). When the suspend is the result of the watchdog timeout, the handler forces an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

In regards to claim 3,6, 9, and 12, Mito discloses the claim limitations as discussed above. Mito further discloses resuming normal operations after performing the error recovery instruction. Mito discloses a resume handler (see figure 7 and column 9 lines 15-27)

In regards to claim 13, Mito discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

self-quiesce logic, coupled to a timer, the self-quiesce logic receiving an error recovery instruction. Mito discloses receiving an interrupt (see figure 4 and column 8 lines 36-37).

a timer for determining when to force execution of the error recovery instruction. Mito discloses a watchdog timeout (see figure 4 item 172 and column 8 lines 36-37).

wherein the self-quiesce logic initiates the timer when the error recovery instruction is received, begins to monitor processor status to determine a time to perform the error recovery instruction. Mito discloses monitoring for interrupts to initiate a suspend routine (see figure 4 and column 8 lines 25-30 and 45-47).

performs the error recovery instruction when the monitoring determines a time for performing the error recovery. Mito discloses initiating a suspend routine (see column 8 lines 45-47).

In regards to claim 14, Mito discloses the claim limitations as discussed above. Mito further discloses the self-quiesce logic forces an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction. Mito discloses high temperatures and low battery, which could represent time to perform error recovery instructions (see figure 4 items 174,176 and column 8 lines 25-30). Mito

further discloses a watchdog timeout, indicating a timeout task (see figure 4 item 172 and column 8 lines 25-30). When the suspend is the result of the watchdog timeout, the handler forces an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

In regards to claims 15 and 18, Mito discloses the claim limitations as discussed above. Mito further discloses wherein the self-quiesce logic allows resuming normal operations after performing the error recovery instruction. Mito discloses a resume handler (see figure 7 and column 9 lines 15-27).

In regards to claim 19, Mito discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

a processor for executing instructions (see column 5 lines 26-30).

self-quiesce logic, coupled to the processor, the self-quiesce logic detecting an error recovery instruction, wherein the self-quiesce logic monitors processor status to determine a time to perform the error recovery instruction. Mito discloses monitoring for interrupts to initiate a suspend routine (see figure 4 and column 8 lines 25-30 and 45-47).

performs the error recovery instruction when the monitoring determines a time for performing the error recovery. Mito discloses initiating a suspend routine (see column 8 lines 45-47).

In regards to claim 20, Mito discloses the claim limitations as discussed above. Mito further discloses the self-quiesce logic forces an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery

instruction. Mito discloses high temperatures and low battery, which could represent time to perform error recovery instructions (see figure 4 items 174,176 and column 8 lines 25-30). Mito further discloses a watchdog timeout, indicating a timeout task (see figure 4 item 172 and column 8 lines 25-30). When the suspend is the result of the watchdog timeout, the handler forces an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

In regards to claims 21 and 24, Mito discloses the claim limitations as discussed above. Mito further discloses wherein the self-quiesce logic allows resuming normal operations after performing the error recovery instruction. Mito discloses a resume handler (see figure 7 and column 9 lines 15-27).

In regards to claims 25 and 26, Mito discloses a method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction. Mito discloses receiving an interrupt (see figure 4 and column 8 lines 36-37)

beginning a timeout task. Mito discloses a watchdog timeout (see figure 4 item 172 and column 8 lines 36-37).

monitoring processor status to determine a time to perform the error recovery instruction Mito discloses monitoring for interrupts to initiate a suspend routine (see figure 4 and column 8 lines 25-30 and 45-47).

performing the error recovery instruction when the monitoring determines a time for performing the error recovery Mito discloses initiating a suspend routine (see column 8 lines 45-47).

In regards to claim 27, Mito discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

means for receiving an error recovery instruction

means for determining when to force execution of the error recovery instruction. Mito discloses initiating a suspend routine (see column 8 lines 45-47).

wherein the means for receiving an error recovery instruction initiates the timer when the error recovery instruction is received. Mito discloses a watchdog timer (see figure 4 item 172 and column 8 lines 36-37).

begins to monitor processor status to determine a time to perform the error recovery instruction. Mito discloses monitoring for interrupts to initiate a suspend routine (see figure 4 and column 8 lines 25-30 and 45-47).

performs the error recovery instruction when a time for performing the error recovery is determined. Mito discloses initiating a suspend routine (see column 8 lines 45-47).

In regards to claim 28, Mito discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

means for executing instructions (see column 5 lines 26-30).

means, coupled to the means for executing instructions, for detecting an error recovery instruction. Mito discloses detecting an interrupt (see figure 4 and column 8 lines 36-37).

monitoring processor status to determine a time to perform the error recovery instruction. Mito discloses monitoring for interrupts to initiate a suspend routine (see figure 4 and column 8 lines 25-30 and 45-47).

performing the error recovery instruction when a time for performing the error recovery is determined. Mito discloses initiating a suspend routine (see column 8 lines 45-47).

Claim 7,10-12,19,22-24,26, and 28 rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,974,147 of Hanrahan et al. referred hereinafter Hanrahan.

In regards to claim 7, Hanrahan discloses a program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 line 13-14).

monitoring processor status to determine a time to perform the error recovery instruction. Hanrahan discloses sequencing to a known state when all current operations that have been started finish (see column 9 lines 20-22).

performing the error recovery instruction when the monitoring determines a time for performing the error recovery. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

In regards to claim 10, Hanrahan discloses the claim limitations as discussed above. Hanrahan further discloses

monitoring a processor interface for an idle condition. Hanrahan discloses receiving an QUIESCE signal to initiate a quiesce function on an I/O control processor (see column 6 lines 58-63 and column 9 lines 15-21). The processor interface must not be busy in order to receive the signal, indicating an idle condition.

withholding access to the processor interface when the idle condition is detected. Hanrahan discloses the QUIESCE signal is provided to suspend further grants of the I/O control processor (see column 6 lines 65-67).

after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle. Hanrahan discloses waiting for all operations to complete before sequencing to a known state (see column 9 lines 15-20).

identifying the time to perform the error recovery instruction when all data transfer paths are idle. Hanrahan discloses sequencing to a known state when all current operations that have completed (see column 9 lines 15-22).

In regards to claim 11, Hanrahan discloses the claim limitations as discussed above. Hanrahan further discloses resuming normal operations after performing the error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 12, Hanrahan discloses the claim limitations as discussed above. Hanrahan further discloses resuming normal operations after performing the error recovery

instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 19, Hanrahan discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

a processor for executing instructions (see column 3 lines 17-20).

self-quiesce logic, coupled to the processor, the self-quiesce logic detecting an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 lines 13-14).

wherein the self-quiesce logic monitors processor status to determine a time to perform the error recovery instruction. Hanrahan discloses sequencing to a known state when all current operations that have been started finish (see column 9 lines 20-22).

performs the error recovery instruction when the monitoring determines a time for performing the error recovery. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

In regards to claim 22, Hanrahan discloses the claim limitations as discussed above. Hanrahan further discloses

wherein the self-quiesce logic monitors processor status to determine a time to perform the error recovery instruction by monitoring a processor interface for an idle condition. Hanrahan discloses receiving a QUIESCE signal to initiate a quiesce function on an I/O control processor (see column 6 lines 58-63 and column 9 lines 15-21). The processor interface must not be busy in order to receive the signal, indicating an idle condition.

withholding access to the processor interface when the idle condition is detected. Hanrahan discloses the QUIESCE signal is provided to suspend further grants of the I/O control processor (see column 6 lines 65-67).

after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle. Hanrahan discloses waiting for all operations to complete before sequencing to a known state (see column 9 lines 15-20).

identifying the time to perform the error recovery instruction when all data transfer paths are idle. Hanrahan discloses sequencing to a known state when all current operations that have completed (see column 9 lines 15-22).

In regards to claim 23, Hanrahan discloses the claim limitations as discussed above. Hanrahan further discloses wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 24, Hanrahan discloses the claim limitations as discussed above. Hanrahan further discloses wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 26, Hanrahan discloses a method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 lines 13-14).

monitoring processor status to determine a time to perform the error recovery instruction. Hanrahan discloses sequencing to a known state when all current operations that have been started finish (see column 9 lines 20-22).

performing the error recovery instruction when the monitoring determines a time for performing the error recovery. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

In regards to claim 28, Hanrahan discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

means for executing instructions (see column 3 lines 17-20).

means, coupled to the means for executing instructions, for detecting an error recovery instruction Hanrahan discloses a receiving a quiesce signal (see column 9 lines 13-14).

monitoring processor status to determine a time to perform the error recovery instruction. Hanrahan discloses sequencing to a known state when all current operations that have been started finish (see column 9 lines 20-22).

performing the error recovery instruction when a time for performing the error recovery is determined. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6,8,9,13-18,20,21,25, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Hanrahan in view of US Patent No. 6,543,002 of Kahle et al. referred hereinafter "Kahle".

In regards to claim 1, Hanrahan discloses a program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 line 13-14).

monitoring processor status to determine a time to perform the error recovery instruction. Hanrahan discloses sequencing to a known state when all current operations that have been started finish (see column 9 lines 20-22).

performing the error recovery instruction when the monitoring determines a time for performing the error recovery. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

However, Hanrahan fails to disclose:

beginning a timeout task;

Kahle disclose a hang detection unit for recovering from a hang condition via a hang recovery sequence. Kahle further discloses a hang condition is determined when the maximum

number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating a timeout task.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hanrahan and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded, thus indicating a timeout task. A person of ordinary skill in the art would have been motivated to combine the teachings because Hanrahan is concerned with recovering from system errors (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables recovery from errors resulting from hang conditions (see column 6 lines 40-45).

In regards to claim 2, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Kahle further discloses forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction. Kahle discloses performing a hang recovery sequence to recover from hang conditions when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45).

In regards to claim 3, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses resuming normal operations after performing the error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 4, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses

monitoring a processor interface for an idle condition. Hanrahan discloses receiving an QUIESCE signal to initiate a quiesce function on an I/O control processor (see column 6 lines 58-63 and column 9 lines 15-21). The processor interface must not be busy in order to receive the signal, indicating an idle condition.

withholding access to the processor interface when the idle condition is detected. Hanrahan discloses the QUIESCE signal is provided to suspend further grants of the I/O control processor (see column 6 lines 65-67).

after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle. Hanrahan discloses waiting for all operations to complete before sequencing to a known state (see column 9 lines 15-20).

identifying the time to perform the error recovery instruction when all data transfer paths are idle. Hanrahan discloses sequencing to a known state when all current operations that have completed (see column 9 lines 15-22).

In regards to claim 5, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses resuming normal operations after performing the error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 6, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses resuming normal operations after performing the

error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 8, Hanrahan discloses the claim limitations as discussed above.

However, Hanrahan fails to disclose beginning a timeout task after receiving the error recovery instruction and forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

Kahle discloses determining when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded for a hang condition (see column 6 lines 40-45), indicating a timeout task. Kahle further disclose a hang detection unit for performing a hang recovery sequence to recover from hang conditions when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hanrahan and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded, thus indicating a timeout task after receiving the error recovery instruction and forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction. A person of ordinary skill in the art would have been motivated to combine the teachings because

Hanrahan is concerned with recovering from system errors (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables recovery from errors resulting from hang conditions (see column 6 lines 40-45).

In regards to claim 9, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses resuming normal operations after performing the error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 13, Hanrahan discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

self-quiesce logic receiving an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 line 13-14).

begins to monitor processor status to determine a time to perform the error recovery instruction. Hanrahan discloses sequencing to a known state when all current operations that have been started finish (see column 9 lines 20-22).

performs the error recovery instruction when the monitoring determines a time for performing the error recovery. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

However, Hanrahan fails to explicitly disclose:

a timer for determining when to force execution of the error recovery instruction, wherein the self-quiesce logic initiates the timer when the error recovery instruction is received.

Kahle disclose a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating a timer for determining when to force execution of the error recovery instruction, wherein the self-quiesce logic initiates the timer when the error recovery instruction is received.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hanrahan and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded, thus indicating a timer for determining when to force execution of the error recovery instruction, wherein the self-quiesce logic initiates the timer when the error recovery instruction is received. A person of ordinary skill in the art would have been motivated to combine the teachings because Hanrahan is concerned with recovering from system errors (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables recovery from errors resulting from hang conditions (see column 6 lines 40-45).

In regards to claim 14, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Kahle further discloses wherein the self-quiesce logic forces an execution of the error recovery instruction when the timer expires before the self-quiesce logic determines a time to perform the error recovery instruction. Kahle discloses performing a hang recovery sequence

to recover from hang conditions when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45).

In regards to claim 15, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 16, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses

wherein the self-quiesce logic monitors processor status to determine a time to perform the error recovery instruction by monitoring a processor interface for an idle condition. Hanrahan discloses receiving an QUIESCE signal to initiate a quiesce function on an I/O control processor (see column 6 lines 58-63 and column 9 lines 15-21). The processor interface must not be busy in order to receive the signal, indicating an idle condition.

withholding access to the processor interface when the idle condition is detected, after access to the processor interface is withheld Hanrahan discloses the QUIESCE signal is provided to suspend further grants of the I/O control processor (see column 6 lines 65-67).

interrogating all data transfer paths to determine when all the data paths are idle. Hanrahan discloses waiting for all operations to complete before sequencing to a known state (see column 9 lines 15-20).

identifying the time to perform the error recovery instruction when all data transfer paths are idle. Hanrahan discloses sequencing to a known state when all current operations that have completed (see column 9 lines 15-22).

In regards to claim 17, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 18, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 20, Hanrahan discloses the claim limitations as discussed above. However, Hanrahan fails to explicitly disclose:

a timer for determining when to abort the monitoring of processor status and data path activity and cause an execution of the error recovery instruction.

Kahle disclose a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating a timer for determining when to abort the monitoring of processor status and data path activity and cause an execution of the error recovery instruction.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hanrahan and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of

completion valid signal is exceeded (see column 6 lines 40-45), thus indicating a timer for determining when to abort the monitoring of processor status and data path activity and cause an execution of the error recovery instruction. A person of ordinary skill in the art would have been motivated to combine the teachings because Hanrahan is concerned with recovering from system errors (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables recovery from errors resulting from hang conditions (see column 6 lines 40-45).

In regards to claim 21, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 25, Hanrahan in view of Kahle discloses a method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 line 13-14).

monitoring processor status to determine a time to perform the error recovery instruction. Hanrahan discloses sequencing to a known state when all current operations that have been started finish (see column 9 lines 20-22).

performing the error recovery instruction when the monitoring determines a time for performing the error recovery. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

However, Hanrahan fails to disclose:

beginning a timeout task;

Kahle disclose a hang detection unit for recovering from a hang condition via a hang recovery sequence. Kahle further discloses a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating a timeout task.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hanrahan and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded, thus indicating a timeout task. A person of ordinary skill in the art would have been motivated to combine the teachings because Hanrahan is concerned with recovering from system errors (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables recovery from errors resulting from hang conditions (see column 6 lines 40-45).

In regards to claim 27, Hanrahan in view of Kahle discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

means for receiving an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 line 13-14).

wherein the means for receiving the error recovery instruction begins to monitor processor status to determine a time to perform the error recovery instruction. Hanrahan

discloses sequencing to a known state when all current operations that have been started finish (see column 9 lines 20-22).

performs the error recovery instruction when a time for performing the error recovery is determined. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

However, Hanrahan fails to disclose:

initiating the timer when the error recovery instruction is received and means for determining when to force execution of the error recovery instruction.

Kahle discloses determining when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded for a hang condition (see column 6 lines 40-45), indicating initiating the timer when the error recovery instruction is received. Kahle further disclose a hang detection unit for performing a hang recovery sequence to recover from hang conditions when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating means for determining when to force execution of the error recovery instruction.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hanrahan and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded, thus indicating initiating the timer when the error recovery instruction is received and means for determining when to force execution of the error recovery instruction. A person of ordinary skill in the art would have been motivated to combine the

teachings because Hanrahan is concerned with recovering from system errors (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables recovery from errors resulting from hang conditions (see column 6 lines 40-45).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C. Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Examiner
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